

CLAIMS

What is claimed is:

1 1. A transmitter coupled to at least two single-channel links of a high-bandwidth

2 link, the transmitter comprising:

3 at least two registers each associated with a single channel link and each receiving a

4 portion of user data provided to the transmitter from a module; and

5 a framer providing i) the user data from the module as a packet having a packet

6 delineator and based on a packet format, and ii) the packet delineator on a particular single-

7 channel link; and

8 wherein one register provides a portion of the packet with the packet delineator to a

9 particular single-channel link, and each register provides a corresponding portion of the packet

10 to an associated single-channel link.

1 2. The invention as recited in claim 1, wherein, for a sequence of packets, the

2 transmitter inserts inter-packet fill to provide the packet delineator of each packet on the

3 particular single-channel link.

1 3. The invention as recited in claim 1, wherein at least one single-channel link is a

2 serial link.

1 4. The invention as recited in claim 3, wherein the serial link is an 8B/10B encoded

2 link operating in accordance with either a Ethernet standard, a Fibre-channel standard, or a

3 Infiniband standard.

1 5. The invention as recited in claim 3, wherein the serial link applies scrambling to

2 the packet including the user data.

1 6. The invention as recited in claim 3, wherein the serial link operates in accordance

2 with a SONET standard.

1 7. The invention as recited in claim 1, wherein the at least two single-channel links

2 are parallel links.

1 8. The invention as recited in claim 7, wherein the parallel links operate in

2 accordance with either a PCI bus standard or a RapidIO standard.

1 9. The invention as recited in claim 1, wherein the transmitter operates in a node in
2 accordance with an asynchronous transfer mode standard or a synchronous optical network
3 standard.

1 10. The invention as recited in claim 1, wherein the transmitter is embodied in an
2 integrated circuit.

1 11. A receiver generating user data for a module from a packet received from at least
2 two single-channel links forming a high-bandwidth link, the receiver comprising:

3 at least two registers each receiving a portion of the packet, wherein

4 one register provides a portion of the packet with a packet delineator from a
5 particular single channel link, and each register provides a corresponding portion of the
6 packet from an associated single-channel link; and

7 a framer that 1) forms the packet from the packet delineator and 2) extracts the user data
8 based on a packet format.

1 12. The invention as recited in claim 11, wherein the packet format includes
2 information in at least one message channel other than the user data.

1 13. The invention as recited in claim 11, wherein the packet format includes error
2 detection or error detection/correction information.

1 14. The invention as recited in claim 13, wherein the error detection or error
2 detection/correction information is cyclic redundancy check information.

1 15. The invention as recited in claim 11, wherein the packet format allows for
2 discarding of inter-packet fill.

1 16. The invention as recited in claim 11, wherein the apparatus operates in a node in
2 accordance with an asynchronous transfer mode standard or a synchronous optical network
3 standard.

1 17. The invention as recited in claim 11, wherein the circuit is embodied in an
2 integrated circuit.

1 18. A method of transmitting user data from a module over at least two single-
2 channel links of a high-bandwidth link, the method comprising the steps of:
3 (a) receiving, in each of at least two registers each having a corresponding single channel
4 link, a portion of user data from the module; and
5 (b) providing 1) the user data as a packet having a packet delineator based on a packet
6 format, and 2) the packet delineator on a particular single-channel link; and
7 wherein one register provides a portion of the packet with the packet delineator to a
8 particular single-channel link, and each register provides a corresponding portion of the packet
9 to an associated single-channel link.

H 1 19. The invention as recited in claim 18, wherein step (b) further includes the step of
G 2 inserting inter-packet fill such that the packet delineator occurs on the particular single-channel
G 3 link for each packet in a sequence of packets.

H 1 20. The invention as recited in claim 18, wherein, for step (b) at least one single-
G 2 channel link is a serial link.

H 1 21. The invention as recited in claim 20, wherein, for step (b) the serial link is an
G 2 8B/10B encoded link operating in accordance with either a Ethernet standard, a Fibre-channel
G 3 standard, or a Infiniband standard.

H 1 22. The invention as recited in claim 20, further including the step of scrambling at
G 2 least one portion of the packet including the user data.

H 1 23. The invention as recited in claim 20, wherein, for step (b), the serial link operates
G 2 in accordance with a SONET standard.

H 1 24. The invention as recited in claim 18, wherein, for step (b) the at least two single-
G 2 channel links are parallel links.

H 1 25. The invention as recited in claim 18, wherein, for step (b) the parallel links
G 2 operate in accordance with either a PCI bus standard or a RapidIO standard.

H 1 26. The invention as recited in claim 18, wherein the method is implemented within a
G 2 node in accordance with an asynchronous transfer mode standard or a synchronous optical
G 3 network standard.

1 27. The invention as recited in claim 18, wherein the method is implemented within a
2 processor of an integrated circuit.

1 28. A method of generating user data for a module from a packet received from at
2 least two single-channel links forming a high-bandwidth link, the method comprising the steps
3 of:

- 4 (a) receiving, in each of at least two registers, a corresponding portion of the packet;
5 (b) providing 1) a portion of the packet with a packet delineator from a particular single
6 channel link, and 2) a corresponding portion of the packet from an associated single-channel
7 link;
- 8 (c) forming the packet from the packet delineator; and
9 (d) extracting the user data based on a packet format.

1 29. The invention as recited in claim 28, wherein step (d) extracts information in at
2 least one message channel other than the user data.

1 30. The invention as recited in claim 28, wherein step (c) forms the packet based on
2 error detection or error detection/correction information included with the packet in accordance
3 with the packet format.

1 31. The invention as recited in claim 30, wherein the error detection or error
2 detection/correction information is cyclic redundancy check information.

1 32. The invention as recited in claim 28, wherein step (c) discards inter-packet fill.

1 33. The invention as recited in claim 28, wherein the method is implemented within a
2 node in accordance with an asynchronous transfer mode standard or a synchronous optical
3 network standard.

1 34. The invention as recited in claim 28, wherein the method is implemented within a
2 processor of an integrated circuit.